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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	2

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,631	WORRELL, FRANK	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 13, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 3 recites the limitation "said first clock signal" in Lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 3 recites the limitation "said slave select signal" in Line 5. There is insufficient antecedent basis for this limitation in the claim.

5. In reference to Claim 13, Examiner is unclear as to how step (C) can "present said command signal a delay after said first clock edge at a slave interface" in response to itself.

6. Claim 15 recites the limitation "said early device select signal" in Line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claim 13 is rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. Claim 13 indicates that in step (C), a command signal is presented a delay after said first clock edge at a slave interface in response to step (C), and therefore indicating that step (C) is dependent upon itself. It is not possible for step (C) to wait until the completion of step (C) to present the command signal as claimed.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 13, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 4,853,847 to Ohuchi ("Ohuchi").

11. In reference to Claim 1, Ohuchi discloses a bus comprising: a master interface configured to (i) receive an early command signal having a predetermined timing relationship to a first clock edge (See Figure 5 'WRRQ') and (ii) present a bus wait signal proximate a second clock edge (See Figure 5 'WAIT'); a slave interface configured to (i) present a command signal a delay after said first clock edge (See Figure 5 'WRRQIO') and (ii) receive a slave wait signal (See Figure 5 'WAITI'); and a control logic configured to (i) register said early command signal to generate said command signal (See Figures 2 and 3 Number 38 and Column 3 Lines 35-53) and (ii) convert said slave wait signal into said bus wait signal (See Figures 2 and 3 Number 38 and Column 3 Lines 56-61).

12. In reference to Claim 13, Ohuchi discloses a method for operating a bus comprising the steps of (A) receiving an early command signal having a predetermined timing relationship to a first clock edge at a master interface (See Figure 5 'WRRQ'); (B) registering said early command signal to generate a command signal in response to step (A) (See Figures 2 and 3 Number 38 and Column 3 Lines 35-53); (C) presenting said command signal a delay after said first clock edge at a slave interface in response to step (C) (See Figure 5 'WRRQIO'); (D) receiving a slave wait signal at said slave interface (See Figure 5 'WAITI'); (E) converting said slave wait signal into a bus wait

signal in response to step (D) (See Figures 2 and 3 Number 38 and Column 3 Lines 56-61); and (F) presenting said bus wait signal at said master interface proximate a second clock edge in response to step (E) (See Figure 5 'WAIT').

13. In reference to Claim 20, Ohuchi discloses a bus comprising: means for receiving an early command signal having a predetermined timing relationship to a first clock edge at a master interface (See Figures 2-5 'WRRQ'); means for registering said early command signal to generate a command signal (See Figures 2 and 3 Number 38 and Column 3 Lines 35-53); means for presenting said command signal a delay after said first clock edge at a slave interface (See Figures 2-5 'WRRQIO'); means for receiving a slave wait signal at said slave interface (See Figures 2-5 'WAITI'); means for converting said slave wait signal into a bus wait signal (See Figures 2 and 3 Number 38 and Column 3 Lines 56-61); and means for presenting said bus wait signal at said master interface proximate a second clock edge (See Figures 2-5 'WAIT').

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 8, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Number 5,291,080 to Amagasaki ("Amagasaki").

16. In reference to Claim 2, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi further teaches that said master interface is further configured to receive an early address signal having said predetermined relationship with said first clock edge (See Figure 2 Number 16), said control logic is further configured to register said early address signal to generate an address signal (See Figure 2 Number 44, Figure 5 'AREG', and Column 4 Lines 37-42), and said slave interface is further configured to present said address signal said delay after said first clock edge (See Figure 5 'AREG'). Ohuchi does not teach that said control logic is further configured to decode said address signal to generate a device select signal and said slave interface is further configured to present said device select signal said delay after said first clock edge. Amagasaki teaches a control unit receiving an address signal, decoding said address signal to produce a device select signal, and presenting said device select signal to the selected device (See Abstract, Figure 1 Number 3, and Column 1 Line 60 – Column 2 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 2, in

order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

17. In reference to Claim 8, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said control logic comprises an address decoder configured to generate a plurality of device select signals responsive to an address signal. Amagasaki teaches a control unit receiving an address signal and decoding said address signal to produce a plurality of device select signals (See Abstract, Figure 1 Number 3, and Column 1 Line 60 – Column 2 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 8, in order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

18. In reference to Claim 9, Ohuchi and Amagasaki teach the limitations as applied to Claim 8 above. Ohuchi further teaches that the control logic further comprises a plurality of registers (See Figure 3 Numbers 42 and 44) configured to register a plurality of early signals each having said predetermined relationship to said first clock edge to generate a plurality of signals said delay after said first clock edge (See Figure 5 'AREG' and 'DWREG' and Column 4 Lines 37-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 9, in order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

19. In reference to Claim 14, Ohuchi teaches the limitations as applied to Claim 13 above. Ohuchi further teaches receiving an early address signal having said predetermined relationship with said first clock edge at said master interface (See Figure 2 Number 16), registering said early address signal in response to said first clock edge to generate an address signal (See Figure 2 Number 44, Figure 5 'AREG', and Column 4 Lines 37-42), and presenting said address signal at said slave interface said delay after said first clock edge (See Figure 5 'AREG'). Ohuchi does not teach decode said address signal to generate a device select signal in response to generating said address signal; and presenting said device select signal at said slave interface in response to decoding said address signal. Amagasaki teaches a control unit receiving an address signal, decoding said address signal to produce a device select signal, and presenting said device select signal to the selected device (See Abstract, Figure 1 Number 3, and Column 1 Line 60 – Column 2 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 14, in

order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

20. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Amagasaki as applied to Claims 2 and 14 above, and further in view of US Patent Number 5,412,662 to Honma et al. ("Honma").

21. In reference to Claim 3, Ohuchi and Amagasaki teach the limitations as applied to Claim 2 above. Ohuchi and Amagasaki do not teach that said master interface is further configured to receive a no-address signal having said predetermined relationship to said first clock signal and said control logic is further configured to inhibit said slave select signal in response to said no-address signal. Honma teaches receiving a signal, which is equivalent to a no-address signal, that is used by control logic to inhibit a select signal (See Figure 5 Number 3A and Column 6 Lines 35-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the select signal inhibit signal of Honma, resulting in the invention of Claim 3, in order to prevent an overwrite of the data written to the currently selected device (See Column 6 Lines 48-62 of Honma).

22. In reference to Claim 15, Ohuchi and Amagasaki teach the limitations as applied to Claim 14 above. Ohuchi and Amagasaki do not teach receiving a no-address signal

having said predetermined timing relationship to said first clock edge at said master interface; and inhibiting said early device select signal in response to receiving said no-address signal. Honma teaches receiving a signal, which is equivalent to a no-address signal, that is used by control logic to inhibit a select signal (See Figure 5 Number 3A and Column 6 Lines 35-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the select signal inhibit signal of Honma, resulting in the invention of Claim 15, in order to prevent an overwrite of the data written to the currently selected device (See Column 6 Lines 48-62 of Honma).

23. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Number 6,085,261 to McIntyre, Jr. et al. ("McIntyre").

24. In reference to Claim 4, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said master interface is further configured to receive an early burst request signal having said predetermined timing relationship to said first clock edge, said control logic is further configured to register said early burst request signal to generate a burst request signal, and said slave interface is further configured to present said burst request signal said delay after said first clock edge. McIntyre teaches a master device (See Figure 1 Number 5) that sends a burst request signal

(See Figure 2 Number 27) to a control device (See Figure 1 Number 4), which then sends a burst request signal (See Figure 3 Number 26) to a slave device (See Column 3 Lines 9-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the burst request scheme of McIntyre, resulting in the invention of Claim 4, in order to efficiently enhance the performance of a data processing system by reducing access time by allowing multiple transfers in response to a single address prompt (See Column 1 Lines 31-40 of McIntyre).

25. In reference to Claim 16, Ohuchi teaches the limitations as applied to Claim 13 above. Ohuchi does not teach receiving an early burst request signal having said predetermined timing relationship to said first clock edge at said master interface; registering said early burst request signal to generate a burst request signal in response to said first clock edge; and presenting said burst request signal at said slave interface said delay after said first clock edge. McIntyre teaches a master device (See Figure 1 Number 5) that sends a burst request signal (See Figure 2 Number 27) to a control device (See Figure 1 Number 4), which then sends a burst request signal (See Figure 3 Number 26) to a slave device (See Column 3 Lines 9-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the burst request scheme of McIntyre, resulting in the invention of Claim 16, in order to efficiently enhance the

performance of a data processing system by reducing access time by allowing multiple transfers in response to a single address prompt (See Column 1 Lines 31-40 of McIntyre).

26. Claims 5, 6, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Application Publication Number 2001/0010063 to Hirose et al. ("Hirose").

27. In reference to Claim 5, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said master interface is further configured to receive a bus request signal and present a bus grant signal, and said control logic is further configured to arbitrate in response to said bus request signal and generate said bus grant signal. Hirose teaches sending a bus request signal to an arbitrator which then generates a bus grant signal (See Page 4 Paragraph 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 5, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

28. In reference to Claim 6, Ohuchi and Hirose teach the limitations as applied to Claim 5 above. Hirose further teaches completing the arbitration within one clock cycle

and presenting the command signal in the next clock cycle (See Figure 5B and Page 4 Paragraph 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 6, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

29. In reference to Claim 17, Ohuchi teaches the limitations as applied to Claim 13 above. Ohuchi does not teach receiving a bus request signal at said master interface; arbitrating in response to receiving said bus request signal; and generating a bus grant signal in response to arbitrating. Hirose teaches sending a bus request signal to an arbitrator which then generates a bus grant signal (See Page 4 Paragraph 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 17, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

30. In reference to Claim 18, Ohuchi and Hirose teach the limitations as applied to Claim 17 above. Hirose further teaches completing the arbitration within one clock cycle and presenting the command signal in the next clock cycle (See Figure 5B and Page 4 Paragraph 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 18, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

31. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Hirose as applied to Claim 5 above, and further in view of US Patent Number 6,282,583 to Pincus et al. ("Pincus").

32. In reference to Claim 7, Ohuchi and Hirose teach the limitations as applied to Claim 5 above. Ohuchi and Hirose do not teach that said master interface is further configured to receive a lock signal and said control logic is further configured to halt arbitration responsive to said lock signal. Pincus teaches a master interface sending a lock signal (See Column 24 Lines 9-19) to a control logic (See Figure 13A), which then halts arbitration in response to said control logic (See Column 24 Lines 24-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Hirose with the lock signal and arbitration halting of Pincus, resulting in the invention of Claim 7, in order to provide indivisible read-modify-write sequences of memory (See Column 12 Line 66 – Column 13 Line 1 of Pincus).

33. In reference to Claim 19, Ohuchi and Hirose teach the limitations as applied to Claim 17 above. Ohuchi and Hirose do not teach receiving a lock signal at said master interface in response to generating said bus grant signal; and halting arbitration in response to receiving said lock signal. Pincus teaches a master interface sending a lock signal (See Column 24 Lines 9-19) to a control logic (See Figure 13A), which then halts arbitration in response to said control logic (See Column 24 Lines 24-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Hirose with the lock signal and arbitration halting of Pincus, resulting in the invention of Claim 19, in order to provide indivisible read-modify-write sequences of memory (See Column 12 Line 66 – Column 13 Line 1 of Pincus).

34. Claims 10, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Amagasaki as applied to Claim 9 above, and further in view of US Patent Number 5,432,907 to Picazo, Jr. et al. ("Picazo").

35. In reference to Claim 10, Ohuchi and Amagasaki teach the limitations as applied to Claim 9 above. Ohuchi and Amagasaki do not teach that said control logic further comprises an arbitration logic configured to generate a bus grant signal. Picazo teaches a control logic that has bus arbitration logic configured to generate a bus grant signal (See Figure 6B Number 610 and Column 30 Lines 42-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic of Picazo, resulting in the invention of Claim 10, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 of Picazo).

36. In reference to Claim 11, Ohuchi, Amagasaki, and Picazo teach the limitations as applied to Claim 10 above. Picazo further teaches that the control logic comprises a multiplexer configured to multiplex control signals, which are equivalent to the early signals, responsive to the bus grant signal (See Figure 6B Numbers 610, 632, and 640 and Column 31 Lines 1-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic and multiplexer of Picazo, resulting in the invention of Claim 11, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 and Column 31 Lines 35-36 of Picazo).

37. In reference to Claim 12, Ohuchi, Amagasaki, and Picazo teach the limitations as applied to Claim 11 above. Picazo further teaches a multiplexer that selects a write control signal based on the bus grant signal (See Figure 6B Numbers 610, 640, and 650 and Column 31 Lines 25-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic and multiplexers of Picazo, resulting in the invention of Claim 12, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 and Column 31 Lines 35-36 of Picazo) and to allow the devices to be either written or read by the microprocessors (See Column 31 Lines 27-31 of Picazo).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Beginning November 2004, the Examiner's telephone number will be changing to 571-272-3624, and the Examiner's supervisor's telephone number will be changing to 571-272-3632.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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